

CLAIMS

1. An integrated circuit comprising a semiconductor die for wire-bonding to a plurality of conductive traces comprising:
 - 5 a first substrate trace having a first end and a second end;
 - a second substrate trace having a first end, said second substrate trace being laterally aligned with said first substrate trace;
 - a first bonding pad located on said semiconductor die, said first bonding pad coupled to said first end of said second substrate trace using a first wire;
 - 10 a second bonding pad laterally aligned with said first bonding pad and located on said semiconductor die, said second bonding pad coupled to said first end of said first substrate trace using a second wire; and
 - a third substrate trace having a first end, said first end of said third substrate trace coupled to said second end of said first substrate trace using a third wire,
 - 15 wherein said third wire crosses over said second substrate trace.
2. The integrated circuit of claim 1 wherein said third wire crosses over said second substrate trace at a location approximately midway between a first end and a second end of said third wire and approximately midway between said first end and a second end of said second substrate trace.
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3. The integrated circuit of claim 1 wherein the first substrate trace and the third substrate trace have approximately equal surface area.
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4. The integrated circuit of claim 1 wherein at least one aggressor signal generates an interfering magnetic field, said interfering magnetic field generating a first magnetic flux between said first substrate trace and said second substrate trace, said interfering magnetic field generating a second magnetic flux between said second substrate trace and said third substrate trace, said first magnetic flux canceling out a substantial portion of said second magnetic flux.
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5. The integrated circuit of claim 1, wherein at least one of said first substrate trace, said second substrate trace, and said third substrate trace are made of copper or tungsten.

6. An integrated circuit comprising a semiconductor die for wire-bonding to a plurality of conductive traces comprising:

5 a first substrate trace having a first end and a second end;

10 a second substrate trace having a first end and a second end, said second substrate trace being laterally aligned with said first substrate trace;

15 a first bonding pad located on said semiconductor die, said first bonding pad coupled to said first end of said second substrate trace using a first wire;

20 a second bonding pad laterally aligned with said first bonding pad and located on said semiconductor die, said second bonding pad coupled to said first end of said first substrate trace using a second wire;

25 a third substrate trace having a first end, said first end coupled to said second end of said second substrate trace using a third wire; and

30 a fourth substrate trace having a first end, said fourth substrate trace being laterally aligned with said third substrate trace, said first end of said fourth substrate trace coupled to said second end of said first substrate trace using a fourth wire, wherein said third wire crosses said fourth wire.

7. The integrated circuit of claim 6 wherein said third wire and said fourth wire cross at a location approximately midway between a first end and a second end of said third wire and a first end and a second end of said fourth wire.

8. The integrated circuit of claim 6 wherein said first substrate trace, said second substrate trace, said third substrate trace, and said fourth substrate trace have approximately equal surface area.

9. The integrated circuit of claim 6 wherein at least one aggressor signal generates an interfering magnetic field, said interfering magnetic field generating a first magnetic flux between said first substrate trace and said second substrate trace, said interfering magnetic field generating a second magnetic flux between said third substrate trace and said fourth substrate trace, said first magnetic flux canceling out a substantial portion of said second magnetic flux.

10. The integrated circuit of claim 6 wherein the lengths of said third wire and said fourth wire are approximately equal.
- 5 11. The integrated circuit of claim 6, further comprising a fifth substrate trace having a first end, said first end of said fifth substrate trace coupled to a second end of said fourth substrate trace using a fifth wire, a sixth substrate trace having a first end, said sixth substrate trace being laterally aligned with said fifth substrate trace, said first end of said sixth substrate trace coupled to a second end of said third substrate trace using a sixth wire, wherein said fifth wire crosses said sixth wire.
- 10 12. The integrated circuit of claim 11 wherein surface areas of said first substrate trace, said second substrate trace, said third substrate trace, said fourth substrate trace, said fifth substrate trace, and said sixth substrate trace are approximately equal.
- 15 13. An integrated circuit comprising a semiconductor die for wire-bonding to a plurality of conductive traces comprising:
 - a first substrate trace having a first end;
 - a second substrate trace having a first end, said second substrate trace laterally aligned with said first substrate trace;
 - 20 a first intervening substrate trace located between said first substrate trace and said second substrate trace, said first intervening substrate trace having a first end;
 - a first bonding pad located on said semiconductor die, said first bonding pad coupled to said first end of said second substrate trace using a first wire;
 - a second bonding pad laterally aligned with said first bonding pad and located on said semiconductor die, said second bonding pad coupled to said first end of said first substrate trace using a second wire;
 - 25 a first intervening bonding pad located between said first bonding pad and said second bonding pad, said first intervening bonding pad coupled to said first end of said first intervening substrate trace using a third wire, wherein said first wire crosses said second wire over said third wire.
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14. The integrated circuit of claim 13, wherein said first wire and said second wire cross at a location approximately midway between a first end and a second end of said first wire and a first end and a second end of said second wire.
- 5 15. The integrated circuit of claim 14, wherein said first wire and said second wire are separated by a separation material, said separation material preventing direct contact between said first wire and said second wire.
- 10 16. The integrated circuit of claim 14, wherein said first wire and said second wire have approximately a same length.
17. The integrated circuit of claim 14, wherein at least one of said first substrate trace, said second substrate trace, and said first intervening substrate trace are made of copper or tungsten.
- 15 18. A method of forming an integrated circuit comprising providing a semiconductor die for wire-bonding to a plurality of conductive traces comprising:
 - providing a first substrate trace, said first substrate trace having a first end;
 - providing a second substrate trace, said second substrate trace having a first end;
 - 20 laterally aligning said second substrate trace with said first substrate trace;
 - providing a first bonding pad on said semiconductor die;
 - coupling said first bonding pad to said first end of said second substrate trace using a first wire;
 - providing a second bonding pad on said semiconductor die;
 - 25 laterally aligning said second bonding pad to said first bonding pad; and
 - coupling said second bonding pad to said first end of said first substrate trace using a second wire, said second wire crossing said first wire.
19. The method of forming an integrated circuit as in claim 18 further comprising crossing said first wire and said second wire at a location approximately midway between a first end and a second end of said first wire and a first end and a second end of said second wire.
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20. The method of forming an integrated circuit as in claim 19 wherein said first substrate trace and said second substrate trace are of equal dimensions, at least one of said first substrate trace and said second substrate trace is comprised of copper or tungsten, and said first wire and said second wire are of equal length.